WHAT IS CLAIMED IS:

1. A method of charging a signal in a semiconductor memory device, wherein:

the semiconductor memory device comprises first and second voltage sources that have at least one different charging characteristic from each other;

the semiconductor memory device performs first and second cycles each of which comprises steps of charging the signal by the first voltage source, switching from the first voltage source to the second voltage source, and charging the signal by the second voltage source after the switching step; and

at least one of a first time period, for which the first voltage source charges the signal, and a second time period, for which the second voltage source charges the signal, in the first cycle is different from that/those in the second cycle.

2. The method claimed in claim 1, wherein the charging characteristic is at least one of power consumption for charging the signal and charging speed for charging the signal.

3. The method claimed in claim 1, wherein the first cycle is the sense cycle of the semiconductor memory device, and the second cycle is the pre-charging cycle of the semiconductor memory device.

4. The method claimed in claim 3, wherein the first time period in the first cycle is shorter than that in the second cycle.

5. The method claimed in claim 4, wherein the first voltage source is an external voltage source of the semiconductor memory device, and the second voltage source is an internal voltage source of the semiconductor memory device.

6. The method claimed in claim 5, wherein the second voltage source is the step-up voltage sourc .

7. A circuit for charging a signal in a semiconductor memory device, wherein:

the semiconductor memory device comprises first and second voltage sources that have at least one different charging characteristic from each other;

the semiconductor memory device performs first and second cycles each of which comprises steps of charging the signal by the first voltage source, switching from the first voltage source to the second voltage source, and charging the signal by the second voltage source after the switching step; and

at least one of a first time period, for which the first voltage source charges the signal, and a second time period, for which the second voltage source charges the signal, in the first cycle is different from that/those in the second cycle.

8. The circuit claimed in claim 7, wherein the charging characteristic is at least one of power consumption for charging the signal and charging speed for charging the signal.

9. The circuit claimed in claim 7, wherein the first cycle is the sense cycle of the semiconductor memory device, and the second cycle is the pre-charging cycle of the semiconductor memory device.

10. The circuit claimed in claim 9, wherein the first time period in the first cycle is shorter than that in the second cycle.

11. The circuit claimed in claim 10, wherein the first voltage source is an external voltage source of the semiconductor memory device, and the second voltage source is an internal voltage source of the semiconductor memory device.

12. The circuit claimed in claim 11, wherein the second voltage source is the step-up voltage source.

13. The circuit claimed in claim 7, wherein the s miconductor

memory device comprises sense amplifiers each of which is connected to two cells, comprising a timing circuit for changing the time instance to perform the switching step in response to a selecting signal for selecting one of the two cells.

14. The circuit claimed in claim 13, wherein the timing circuit comprises at least one capacitor one of whose terminals is connected to the selecting signal.

15. The circuit claimed in claim 13, wherein the timing circuit comprises a NOR circuit one of whose inputs is connected to the selecting signal.

16. A semiconductor memory device comprising the circuit claimed in claim 7.